REMARKS

Please cancel Claims 2 and 5 without prejudice. New Claims 21-28 are added. Claims 1, 3, 18 and 20-28 are pending. Claims 3, 18 and 20 are amended. No new matter is added by the claim amendments. Support for the claim amendments can be found in Figures 6c and 11 of the application and in the discussion of those figures.

Claims 18 and 20 are allowed. (The Summary page of the Office Action identifies Claim 20 as being allowed; however, on page 6 of the Office Action, Claim 19 is identified as being allowed. Claim 19 has been previously canceled, and Applicants believe that the reference on page 6 should be to Claim 20, particularly in view of the allowance of Claim 18 from which Claim 20 depends.) Applicants thank the Examiner for allowing Claims 18 and 20.

Claim Objections

Claims 2 and 5 were objected to under 37 CFR § 1.56 as being redundant and as not further limiting Claim 1. Claims 2 and 5 are canceled herein, rendering the objection moot.

35 U.S.C. § 103(a)

The instant Office Action states that Claims 1 and 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Application No. 02-054058 by Koichi in view of United States Patent No. 5,437,017 by Moore et al. ("Moore"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention recited in Claims 1 and 3 are patentable over Koichi and Moore, alone or in combination.

Applicants respectfully submit that Koichi does not show or suggest an indication that a target instruction has been translated into a host instruction, as recited in the claims. Specifically, Applicants respectfully submit that Koichi does not show or suggest "means for providing an indication whether a first memory address to be written stores a target instruction which has been translated to at least one host instruction that is stored at a second memory address as recited in independent Claim 1.

The claimed indication is associated with a memory address for a target instruction that has been translated into a host instruction, but nevertheless the claimed indication is an indication that a target instruction has been so translated. The claimed indication maintains coherency between a target instruction and a host instruction translated from that target instruction, in essence by preventing the target instruction from being overwritten before the host instruction is updated, invalidated or removed.

As understood by the Applicants, Koichi shows only converting an exclusive instruction code to a general instruction code. There is no mention of the claimed indication.

Applicants respectfully submit that Moore does not overcome the shortcomings of Koichi. As understood by the Applicants, Moore only maintains coherency between a virtual address and a physical address translated from the virtual address. At best, Moore's translation lookaside buffer invalidate (TLBI) instruction appears to suggest an indication that an entry within the translation

lookaside buffer (TLB) is invalid. That is, at best, Moore can perhaps be read as providing an indication whether the translation between a virtual address and a physical address is valid or invalid. However, the claimed indication is not concerned with the translation between a virtual address and a physical address. As noted above, the claimed indication pertains to the translation between a target instruction and a host instruction.

In summary, Applicants respectfully submit that Koichi and Moore, alone or in combination, do not show or suggest "means for providing an indication whether a first memory address to be written stores a target instruction which has been translated to at least one host instruction that is stored at a second memory address" as recited in independent Claim 1.

Therefore, Applicants respectfully submit that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is traversed and that Claim 1 is in condition for allowance.

Claim 3 includes all of the limitations of Claim 1 plus additional limitations. Accordingly, Applicants respectfully submit that the basis for rejecting Claim 3 under 35 U.S.C. § 103(a) is also traversed and that Claim 3 is in condition for allowance.

Conclusions

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1 and 3 overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

MURABITO HAO & BARNES L.L.P.

Dated: 01/12/ 2009

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